A design-of-experiments approach to maximize the reliability of adjustable speed drives

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Un diseño de experimentos enfocado a maximizar la confiabilidad de *drives* de velocidad ajustable

***Abstract*— There are several proposals to improve the reliability of adjustable speed drives. One is to use an active rectifier and a small-valued capacitor. Another is to use switching patters aimed at reducing the current ripple flowing through the capacitor. A third one is to closely monitor the capacitors, in order to detect its degradation. Manufacturers claim, however, that modern capacitors can perform satisfactorily in this application. This paper presents a methodology to select the design specifications for a standard ASD, in such a way that the capacitor operational life can be maximized. It is based on the design of experiments technique, a statistical tool whose advantage is that the parameters with the highest impact on the operational life can easily be identified at the design stage, and dealt with in a systematic manner.**

The selecting procedure of an electrolytic capacitor is already well known, however there is no explicit link between the electrical variables and the variables of reliability. As a solution to this difficulty is presented a method for relating the electrical behavior with the capacitor operational life.

***Keywords*— Reliability, Drives, Design methodology.**

I. INTRODUCTION

For a long time, a major source of concern in adjustable speed drives (Fig.1) has been the large electrolytic capacitor connected across the DC-link. The current flowing through the capacitor includes harmonics produced both by the rectifier at the line side, and the inverter at the load side. The temperature within the capacitor rises as the current flows through the equivalent series resistance (ESR), degrading the capacitor characteristics and shortening the lifespan [1][2].

Several approaches have been followed in order to improve the reliability. One approach is to drastically reduce the capacitor to values so small that either film or ceramic capacitors can be used, instead of electrolytic ones. Although its feasibility has already been demonstrated, this approach requires an active rectifier as the first stage [3]. Furthermore, the complete elimination of capacitors across the DC link can be achieved, but at the expense of a voltage with a high ripple [4]. Besides the obvious complexity of the added hardware, such converters are highly susceptible to transient over or under voltages on the DC link [5]. Even minor grid voltage imbalance can cause a large second harmonic ripple to appear in the link voltage, possibly interfering with the load. These conditions impose higher restrictions on the control system [6].

Since the temperature rise is produced by the current flowing through the ESR, a second approach is to use optimized switching patterns aimed at reducing the current stresses on the capacitors. The drawback, however, is that the requirements of a current with a lower harmonic content sometimes are in conflict with other operational requirements [7][8].

A third approach followed is to closely monitor the capacitors, in order to timely detect its degradation [9]-[11]. This approach does not provide a higher reliability. Instead, it is focused in avoiding catastrophic failures, thus shortening the down time, and providing a better availability.

An ASD for applications not requiring regenerative operation might benefit from the simplest configuration, with an uncontrolled rectifier as front-end. The advantages are that the requirements imposed on the controller block are greatly simplified, and that the reliability attained with a diode-based rectifier is much higher than that exhibited by an active rectifier built with transistors. In fact, several semiconductor manufacturers offer integrated modules containing the uncontrolled rectifier and a three-phase inverter in a single package (shown within the dotted box in Fig. 1). The input and output stages are unconnected, and an LC filter can be connected in between.

The capacitor C_F is the one blamed as the major source of failures. Manufacturers claim, however, that capacitors for this application have longer lives than previously thought [12]. A common reliability prediction procedure is outlined in the MIL HDBK217-F handbook [13]. The manufacturers' argument is that the handbook relies on statistical data collected throughout the years, and such data might not apply to current-technology capacitors, hence yielding misleading reliability predictions. A study recently published seems to confirm the statement [14].

The design procedure for the LC filter is already well known,

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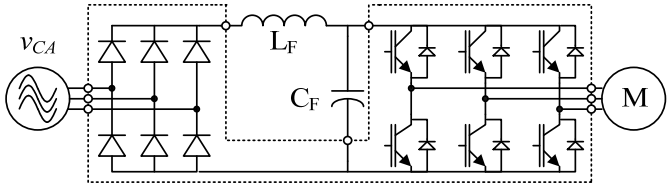

Fig. 1 Standard adjustable speed drive with an electrolytic capacitor in the DC-link.

TABLE I. Expected lifetime for PEH200 electrolytic capacitors, at T_M = 85°C [18]

Diameter (mm)	35	50	65	75	90
L_B (10^3 hours)	20	24	30	40	60

and several guidelines can be followed: specifying the amount of voltage ripple, the cut-off frequency, or the damping factor, among others [15]. The drawback is that the procedure usually employs a desired operating point as input data, without including the capacitor reliability as a design parameter. As a result, the designer does not know what effect a change in the quality factor, for instance, will have on the operational life. There have been a few attempts to provide design criteria that take into account the size and the capacity of the DC-link capacitor [16]. The proposals, however, do not ensure that reliability can be maximized because it is not explicitly included. The most advantageous, least expensive approach is to introduce reliability as early as possible in a product life cycle [17].

This paper presents a methodology to select an operating point that maximizes the capacitor operational life. It is based on the design-of–experiments technique, a statistical tool whose advantage is that the parameters with the highest impact on the operational life, under normal operating conditions, can easily be identified at the design stage. Once the effect of these parameters is identified, the filter can be improved to comply with a reliability target. The analysis is performed for a 5 kW ASD, and four optimization parameters are taken into account: the cut-off frequency f_C, and the quality factor Q of the filter, the capacitor voltage rating V_R, and the carrier frequency f_{PWM} used to modulate the inverter.

II. CAPACITOR OPERATIONAL LIFE

The capacitor operating life can be mathematically described as [12]:

$$L_{OP} = L_B \, f_1(V) \, f_2(\Delta T) \tag{1}$$

where L_B is the expected lifetime at the rated hot-spot temperature T_M, and depends on the capacitor diameter, as can be seen in table I.

The term f_1 takes into account the voltage stress applied to the capacitor, and is given by:

$$f_1(V) = 4.3 - 3.3\frac{V_A}{V_R} \tag{2}$$

where V_A is the voltage applied to the capacitor, and V_R is the rated voltage. In turn, f_2 is a function of the internal temperature rise, and is expressed as:

$$f_2(\Delta T) = 2^{(TM - Th)/B} \tag{3}$$

where B is a constant that depends on the capacitor construction, and T_h is the actual hot-spot temperature. The term T_h depends on the power dissipated by the capacitor which, in turn, depends on the ESR, and on the current flowing through the capacitor. Further, the ESR exhibits a highly nonlinear behavior, as can be noticed in Fig. 2. The plot corresponds to a 4700 μF electrolytic capacitor rated at 450 V [19].

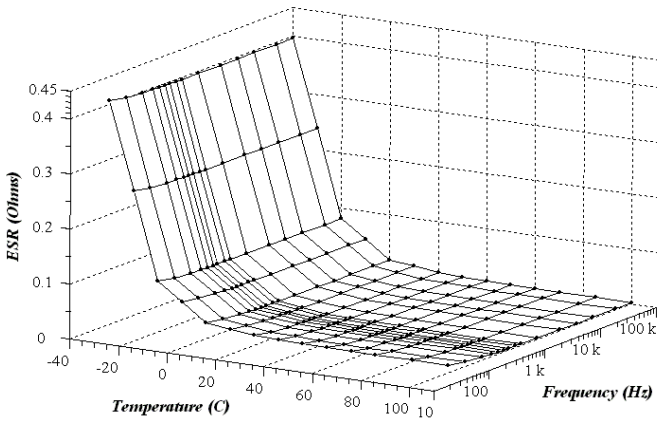

Fig. 2 ESR as a function of the hot-spot temperature, and the frequency.

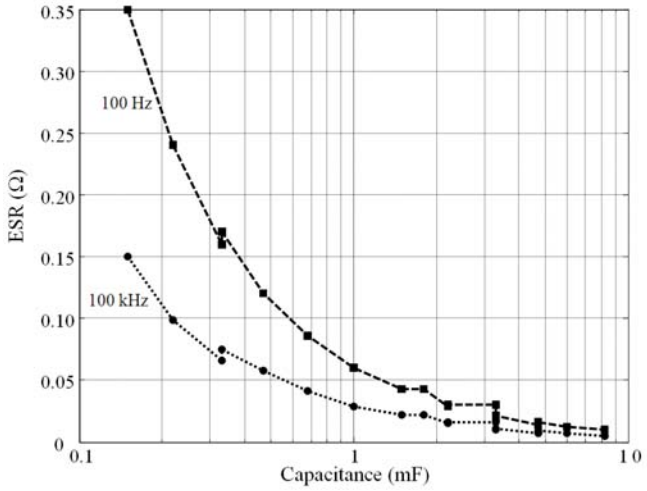

Fig. 3 ESR as a function of the capacitance value.

The ESR also depends on the capacitance value, as can be seen in Fig. 3. The graph corresponds to capacitors rated at 450 V, from the PEH200 family, and shows that the ESR is inversely proportional to the capacitance value. Fig. 4 illustrates the ESR as a function of the rated voltage, for 4700 μF capacitors from the same family. Both graphs correspond to an ambient temperature equal to 20°C.

III. DESIGN-OF-EXPERIMENTS BASED ANALYSIS

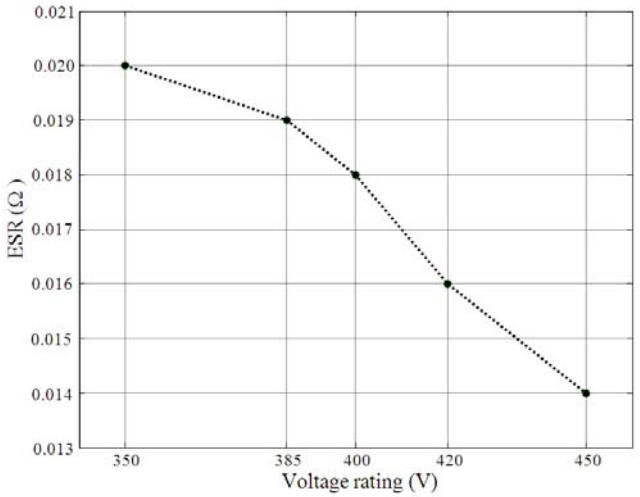

Fig. 4 ESR as a function of the rated voltage.

TABLE II. MINIMUM AND MAXIMUM VALUES OF THE DESIGN PARAMETERS

Parameter	Minimum	Maximum
f_C [Hz]	50	100
Q	2.4	5
V_R [V]	350	450
f_{PWM} [Hz]	900	4500

The Design-of-Experiments (DOE) technique analyzes the simultaneous effect of several factors on an output variable. When properly planned and executed, it helps obtain the maximum amount of information with the minimum amount of work. Using a factorial design all the factors are varied at once, and experiments (or evaluations) are performed for all combinations of levels for all of the factors. This procedure reveals what the effect of one variable is when the other factors are changing.

Interaction occurs when the effect on the response of a change in the level of one factor from low to high depends on the level of another factor. In other words, when an interaction is present between two factors, the combined effect of those two factors on the response variable cannot be predicted from the separate effects. The effect of two factors acting in combination can either be greater (synergy) or less (interference) than would be expected from each factor separately. In a 2-level factorial design, each factor is assigned a minimum and a maximum value. Let n be the number of factors. The 2-level factorial design requires that the experiment be performed $2n$ times. A fractional factorial design requires fewer experiments, and there is a simple relationship for the minimum number of runs required: round up the number of factors to a power of two and then multiply by two [20].

In the current case the output variable is the capacitor operating life, and the factors are the following four design parameters ($n = 4$):

- The cut-off frequency f_C of the filter. It should be low enough to provide a ripple-free DC voltage, and to prevent the backward propagation of the current harmonics generated by the inverter.

- The quality factor Q of the filter. Its value should provide a suitable transient response.

TABLE III. DESIGN MATRIX WITH MINIMUM AND MAXIMUM VALUES

m	f_C [Hz]	Q	V_R [V]	f_{PWM} [kHz]	Lop [10^3 hrs]
1	50	2.4	350	0.9	670
2	50	2.4	450	4.5	1492
3	50	5	350	4.5	326
4	50	5	450	0.9	550
5	100	2.4	350	4.5	657
6	100	2.4	450	0.9	567
7	100	5	350	0.9	70
8	100	5	450	4.5	157

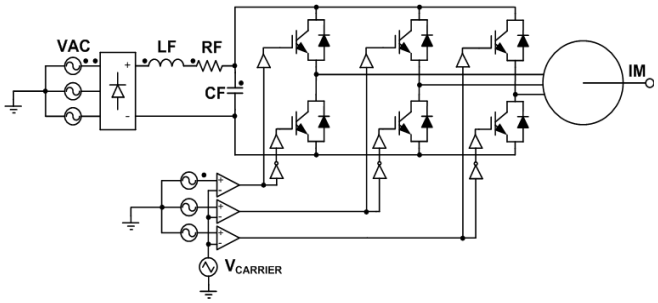

Fig. 5 Circuit schematic.

- The capacitor voltage rating V_R.

- The carrier frequency f_{PWM} used to modulate the inverter. Besides the harmonics at $6\ h\ f_{LINE}$, the current flowing through the capacitor will include components related to this frequency.

According to the DOE technique, it is necessary to select a minimum and a maximum value for each parameter. The selected values are listed in table II. It will be assumed that the voltage at the DC-link is $V_{DC} = 280$ V, the output power is $P_O = 5$ kW, $R_F = R_L/100$, and the ambient temperature is $T_A = 40$C.

A. Design matrix

The first step is to setup an appropriate design matrix, each row containing a different combination of the design parameters. Each combination constitutes an entry, and the operating life will be calculated as many times as entries are in the matrix. Since $n = 4$, if the fractional factorial design strategy is followed, then there are 8 combinations ($m = 8$), as shown in table III**.**

B. Operating life calculation

The inductor and the capacitor are calculated following the procedure described in the previous section, with the input parameters listed in the second and third columns in the design matrix. The resulting circuits are simulated in PSIM using the schematic shown in Fig. 5. A PWM modulation with a triangular carrier is used, and its value is given by the fifth column in the design matrix. The model of a symmetrical 3-phase squirrel-cage induction machine was used in the simulations. The outputs are a set of vectors containing the current flowing through capacitor

TABLE IV. PARTIAL AVERAGES AND SUM OF SQUARES FOR DESIGN PARAMETERS

	f_C [Hz]	Q	V_R [V]	f_{PWM} [kHz]
Avg(max)	363	276	692	658
Avg(min)	760	847	431	464
ΔAvg	-397	-571	260	194
SS	314454	651223	135632	75055

C_F. The current vectors are exported to Matlab, to calculate the hot-spot temperature. following the procedure described in [21].

The inputs for the calculation are the current vector, the ESR matrix for the capacitor, and the corresponding thermal resistance R_θ. The operating life *Lop* is calculated using equations (1), (2) and (3). *Lb,* T_M and *B* are obtained from manufacturer data, and $V_A = V_{DC}$. The results are listed in the rightmost column of the design matrix.

C. Variance analysis

The following procedure follows the guidelines provided by Hicks [22]. The overall arithmetic average $\overline{Lop}$ should be calculated using:

$$\overline{Lop} = \frac{1}{n}\sum_{j=1}^{n} Lop_j \tag{4}$$

For the operational lives listed in the rightmost column, table II, $\overline{Lop}$ = 561.3 x 10^3 hours.

Let *par* represent any of the design parameters. Eight partial averages should be calculated, two for each variable *par*: one with the *Lop* values obtained when the variable is at its maximum, and another with the values obtained when the variable is at its minimum. That is:

$$Avg(max)_{par} = \frac{1}{4}\sum_{j=1}^{4} Lop_j \,|_{par=max} \tag{5}$$

$$Avg(min)_{par} = \frac{1}{4}\sum_{j=1}^{4} Lop_j \,|_{par=min} \tag{6}$$

The difference is:

$$\Delta Avg_{par} = Avg(max)_{par} - Avg(min)_{par} \tag{7}$$

and the corresponding Sum-of-Squares SS_{par} is:

$$SS_{par} = 2\,\Delta Avg_{par}{}^2 \tag{8}$$

The results are listed in table IV. As an example, the *Avg(max)* for f_C is obtained averaging the *Lop* values for rows *m* = 4 through 8 in the design matrix.

As previously stated, the term "interaction" refers to the combined effect of two variables on the output. At this point, the number of interactions n_I is selected considering the non-repetitive, binary combinations of two variables. There are three interactions in an analysis with four variables. The first interaction is "$f_C\,Q$ OR $V_R f_{PWM}$". The second one is "$f_C\,V_R$ OR $Q\,f_{PWM}$". The third is "Q V_R OR $f_C\,f_{PWM}$". Further, there will be a high value H, and a low value L associated with each interaction. Let *int* represent any of the interactions. At this point it is necessary to calculate the same terms that were calculated for the variables. That is:

TABLE V. PARTIAL AVERAGES AND SUM OF SQUARES FOR INTERACTIONS

			Interactions		
m		*Lop* [10^3 hrs]	$f_C\,Q$ OR $V_R f_{PWM}$	$f_C\,V_R$ OR $Q f_{PWM}$	$Q\,V_R$ OR $f_C f_{PWM}$
1	▪▪▪	670	H	H	H
2	▪▪▪	1492	H	L	L
3	▪▪▪	326	L	H	L
4	▪▪▪	550	L	L	H
5	▪▪▪	657	L	L	H
6	▪▪▪	567	L	H	L
7	▪▪▪	70	H	L	L
8	▪▪▪	157	H	H	H
		Avg(H) (10^3)	597	430	508
		Avg(L) (10^3)	525	692	614
		ΔAvg (10^3)	72	-262	-105
		SS (10^6)	10358	137708	22176

$$Avg(max)_{int} = \frac{1}{4}\sum_{j=1}^{4} Lop_j \,|_{int=H} \tag{9}$$

$$Avg(min)_{int} = \frac{1}{4}\sum_{j=1}^{4} Lop_j \,|_{int=L} \tag{10}$$

$$\Delta Avg_{int} = Avg(max)_{int} - Avg(min)_{int} \tag{11}$$

$$SS_{\text{int}} = 2\,\Delta Avg_{\text{int}}{}^2 \tag{12}$$

The numerical results are listed in table V. As an example, the term *Avg(H)* for the interaction $f_C\,Q$ OR $V_R f_{PWM}$ is calculated averaging rows 1, 2, 7 and 8.

The error ε is calculated using:

$$\varepsilon = \sum_{j=1}^{3} (SS_{\text{int}})_j \tag{13}$$

The values listed in table V yield ε = 170242 x 10^6.

There are several degrees of freedom: DF_{par} for parameters, DF_{int} for interactions, and DF_{ε}. for the error. Since each parameter takes only two different values, the following simplifications can be applied: DF_{par} = 1, DF_{int} = 1 and $DF_{\varepsilon} = n_I$ = 3. The next step is to obtain the mean square MS values for the parameters, the interactions, and the error. With the aforementioned simplifications, the mean square value for variables is $MS_{par} = SS_{par}$. The mean square value for interactions is $MS_{int} = SS_{int}$. The mean square value for the error is:

TABLE VI. RATIO F_{PAR} FOR THE DESIGN VARIABLES

	f_C [Hz]	Q	V_R [V]	f_{PWM} [kHz]
F_{par}	5.54	11.48	2.39	1.32

$$MS_{\varepsilon} = \frac{\varepsilon}{DF_{\varepsilon}} = 56750 \times 10^{6} \tag{14}$$

For each parameter, the ratio F_{par} is calculated as:

$$F_{par} = \frac{MS_{par}}{MS_{\varepsilon}} \tag{15}$$

The numerical results are listed in table VI.

Let α represent the level at which the designer is willing to risk in concluding that a significant effect is not present when in actuality it is. The term $F(\alpha,DF_{par},DF_{\varepsilon})$ corresponds to the critical value of the statistical *F*-distribution, and is tabulated in most statistical books [23]. If the calculated F_{par} ratio is greater than the tabulated value of $F(\alpha,DF_{par},DF_{\varepsilon})$, then the parameter does have a significant effect on the operational life, and should be included in the optimization procedure.

Let α = 0.2 (that is, a 20% risk level). The tabulated value is $F(\alpha,DF_{par},DF_{\varepsilon}) = 2.05$. Comparing this value with those listed in table VI, it turns out that $F_{PWM} < 2.05$. Therefore, the modulation frequency has a minor effect on *Lop*, and can be excluded from further consideration. Also, the largest F_{par} corresponds to the variable with the highest impact on the operational life which, in this case, is the quality factor *Q*. Once the variables with the highest impact have been identified, the next step is to find out how should the variables be changed in order to improve *Lop*. The following prediction equation can be used for this purpose:

$$Lop = \overline{Lop} + \sum_{par=1}^{3} \frac{\Delta Avg_{par}}{\mathrm{F}_{(\alpha,\mathrm{DF}_{\mathrm{par}},\mathrm{DF}_{\varepsilon})}} \tag{16}$$

where $\overline{Lop}$ is calculated with equation (4). The summation includes the three terms in table VI larger than $F(\alpha,DF_{par},DF_{\varepsilon})$. Using the previously calculated values:

$$Lop = 561.3 - \frac{397}{2.05}\bigg|_{fC} - \frac{571}{2.05}\bigg|_{Q} + \frac{260}{2.05}\bigg|_{VR}$$

$$Lop = 561.3 - 193_{fC} - 278_{Q} + 127\big|_{VR} \tag{17}$$

To improve the operational life, the variables with positive coefficients should be increased, and the variables with negative coefficients should be reduced. According with these results, in order to improve the capacitor operating life, both the quality factor and the cut-off frequency should be reduced, and the voltage rating should be increased.

IV. DISCUSSION

It is instructive to compare the operational lives obtained with the different design values listed in table VII, representing a gradual optimization procedure. The first row corresponds to the shortest operating life, and will be used as a reference. The rightmost column lists the improvement obtained, when compared with the previous step.

TABLE VII. OPERATIONAL LIVES COMPARISON

f_C [Hz]	Q	V_R [V]	f_{PWM} [kHz]	Lop [10^3 hrs]	ΔLop [10^3 hrs]
100	5	350	900	85	---
100	5	350	4.5	116	33
100	5	450	4.5	157	41
50	5	450	4.5	442	285
50	2.4	450	4.5	1492	1050

The first row corresponds to a worst-case design, and the operational life attained is rather short. In the second row f_{PWM} is increased, up to 4.5 kHz, yielding a 33 x 10^3 hrs improvement in *Lop*. In the third row the voltage rating is increased to 450 V, yielding ΔLop = 41 x 10^3 hrs. In the fourth row the cut-off frequency is halved, and the resulting improvement in *Lop* is much larger. Finally, in the fifth row the quality factor is reduced down to 2.4, and the *Lop* improvement in the largest. Although f_{PWM} was not included in the prediction equation, nevertheless for comparison purposes its effect was included in table VII.

It is apparent that the larger coefficients in the prediction equation yield the larger ΔLop. Therefore, if in a particular application the calculated lifetime of the capacitor does not fulfill the requirements, the best thing to do is to redesign the filter with a smaller quality factor. This will yield a larger capacitor and a smaller inductor (larger capacitors imply lower ESR values, as illustrated by Fig. 3). Designing a filter with a lower *fc* will also produce a higher capacitance value, although in this case a larger inductor is also obtained

Capacitors rated at higher voltages are built in larger cans, thus producing both a reduction in the hot-spot temperature (due to a lower ESR, as shown in Fig. 4), and an increase in the term $f_1(V)$, equation (2).

It must be pointed out that the numerical values presented are for steady state operation, not taking into account the transients that occur during motor start-up. Also, the simulations were performed with a flicker-free well-balanced AC supply. In adjustable speed drives connected to unbalanced supplies the capacitors exhibit a much shorter life, because the unbalance produces low-order current harmonics.

It is worth pointing out that the maximum carrier frequency f_{PWM} used for the calculations was not very high. A higher value can be used, but the numerical results obtained are practically the same. This occurs because, as can be noticed from Fig. 2, the ESR does not change significantly at frequencies above 2 kHz.

In this case in was assumed that f_C, Q, V_R, f_{PWM} were "free" parameters and could be modified at will within reasonable limits. There is no doubt that the output frequency generated by the inverter also affects the operational life. This frequency, however, usually depends on the operating point desired, and cannot be modified at will because it depends on the load requirements. Therefore, variables such as the output frequency must be excluded from the analysis.

It should be noted that the prediction equation does not yield an actual value of the operational life expected. Rather, it represents the magnitude of the impact that each variable has on

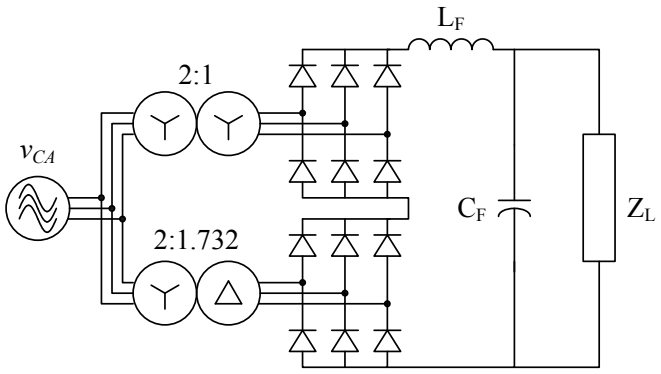

Fig. 6 Adjustable speed drive with a 12-pulse front-end.

Lop. Also, the operational lives calculated are just predictions obtained using statistical data gathered by the manufacturer. The coefficients in equation (17) resemble the sensitivity factors used in other applications, such as the design of analog filters. In order to perform the sensitivity analysis it is necessary to have a mathematical expression relating cause and effect. In many cases the relationship is not straightforward, and it is much easier to apply the method described herein.

The methodology can be applied in a straightforward manner to other configurations, such as the ASD with a 12-pulse front-end illustrated in Fig. 6. To maintain the same voltage level at the DC-link, two step-down voltage transformers were used at the inputs. A filter with a higher cut-off frequency can be used in this circuit, which exhibits the same trends obtained in the prediction equation, but with longer operational lives. As an example, using the values listed in the first row, table VII, yields L_{OP} = 2955 x 10^3 hours. A further advantage of the circuit is the power-factor improvement.

V. CONCLUSIONS

This paper presents a methodology to improve the operational life that can be achieved by an electrolytic capacitor in an adjustable speed drive. The methodology is based on the design-of-experiments technique, and was applied to an ASD rated at 5 kW. The results show that the operational life can be extended by decreasing the cut-off frequency, and the quality factor, and by increasing the voltage rating. The carrier frequency does not have a major effect on the operational life.

Clearly, the same conclusions could be achieved following a heuristic approach. The advantage of the methodology followed herein is that several variables can be dealt with in a systematic manner at the design stage, providing a sturdier design in a much shorter time. The methodology is computationally intensive but, nowadays, that does not represent a major obstacle. It can be applied to other configurations, such as the ASD with a 12-pulse front-end, or an ASD with AC input reactors instead of the inductor at the DC-link.

The MIL HDBK 217F procedure was selected for the reliability calculations because it can be applied without actually building the converter, and is still most widely accepted in the aerospace and military industry, although it is generally viewed as pessimistic.

REFERENCES

[1] W. Sarjeant, I. Clelland, and R. Price, Capacitive Components for Power Electronics, Proceedings of the IEEE, Vol. 89, No. 6, June 2001, pp. 846-855.

[2] P.D. O'Connor. Practical Reliability Engineering. John Wiley and Sons, Chichester, West Sussex, England, 2002, Chapter 9, Electronic systems reliability, pp. 247-289.

[3] Xiong Liu, Peng Wang, Poh Chiang Loh, Blaabjerg, F. and Mingyu Xue, Six switches solution for single-phase AC/DC/AC converter with capability of second-order power mitigation in DC-link capacitor, Energy Conversion Congress and Exposition (ECCE), 2011 IEEE, pp. 1368-1375.

[4] Grabner, C., Electrical drives without DC link converter component and recuperation capability, International Conference on Power Engineering, Energy and Electrical Drives, 2009, POWERENG '09, pp. 128-133.

[5] Maheshwari, R., Munk-Nielsen, S., Henriksen, B., Obel, P.M. and Kragh, H. Active damping technique for small DC-link capacitor based drive system, 2010 IEEE International Symposium on Industrial Electronics (ISIE), pp. 1205- 1209.

[6] G. Hwang, P. Lehn and M. Winkelnkemper, Control of Grid Connected AC-DC Converters with Minimized DC Link Capacitance Under Unbalanced Grid Voltage Condition, 2007 European Conference on Power Electronics and Applications, Aalborg, Denmark 2007, pp. 1-10.

[7] O. Pyrhen, H. Saren, K. Rauma and O. Laakkonen, Verification of Frequency Converter with Small DC-Link Capacitor, EPE2005 Conference proceedings.

[8] M. Huber, W. Amrhein, S. Silber, M. Reisinger, G. Knecht and G. Kastinger, Ripple Current Reduction of DC Link Electrolytic Capacitors by Switching Pattern Optimisation, 36th Annual IEEE Power Electronics Specialists Conference Record, Recife, Brazil, 2005, pp. 1875-1880.

[9] Anderson, J.M., Cox, R.W. and Noppakunkajorn, J., An on-line fault diagnosis method for power electronic drives, 2011 IEEE Electric Ship Technologies Symposium (ESTS), pp. 492- 497.

[10] D.-C. Lee, K.-J. Lee, J.-K. Seok and J.-W. Choi, On-Line Capacitance Estimation of DC-Link Capacitor by Input Current Injection for PWM Converters, EPE 2003, Conference Proceedings.

[11] A. Imam, D. Divan, R. Harley and T. Habetler. Real-Time Condition Monitoring of the Electrolytic Capacitors for Power Electronics Applications, 22nd. IEEE Applied Power Electronics Conference, Anaheim, California, 2007. Pp. 1057-1061.

[12] S. Parler, Reliability of CDE Aluminum Electrolytic Capacitors. Application Note, Cornell-Dubilier Electronics (Available at http://www.cde.com/tech/reliability.pdf)

[13] Department of Defense, *Reliability Prediction of Electronic Equipment*, Military Handbook 217-F, USA, 1991.

[14] D. Hirschmann, D. Tissen, S. Schröder and R. De Doncker. Reliability Prediction for Inverters in Hybrid Electrical Vehicles. IEEE Transactions on Power Electronics, Vol. 22, No. 6, November 2007, pp. 2511-2517.

[15] K. Rajashekara, V. Rajagopalan, A. Sevigny, J. Vithayathil. DC Link Filter Design Considerations in Three-Phase Voltage Source Inverter-Fed Inductor Motor Drive System. IEEE Transactions on Industry Applications. Vol. 23, No. 4, July-August 1987, pp. 673-680.

[16] M. Winkelnkemper and S. Bernet. Design and optimization of the DC-link capacitor of PWM voltage source inverter with active front-end for low-voltage drives. EPE 2003 Conference Proceedings.

[17] Mark Levin and Ted Kalal. "*Improving product Reliability. Strategies and Implementation*". John Wiley and sons. Chichester, England 2003.

[18] PEH200 capacitors data sheet, Evox Rifa.

[19] Capacitor PEH200YV447BM ESR Matrix, Evox Rifa.

[20] J. K. Telford, A Brief Introduction to Design of Experiments. Johns Hopkins APL Technical Digest, Volume 27, Number 3 (2007), pp. 224-232.
[21] M. L. Gasperi, Life Prediction Modeling of Bus Capacitors in AC Variable-Frequency Drives. IEEE Transactions on Industry Applications, Vol. 41, No. 6, November/December 2005, pp. 1430-1435.
[22] C.R. Hicks, *"Fundamental Concepts in the Design of Experiments"* Holt, Rinehart and Winston, Inc, New York, 1982.
[23] J. Wesley Barnes*, "Statistical Analysis for Engineers and Scientists: A computer-based approach",* Mc Graw Hill, 1994, pp. 366.

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